CLAIMS:

1. A method for digital recursive filtering an input signal according to a rational filter transfer function clocked by a clock signal comprising the following steps:

(a) providing first and second order rational functions corresponding to the rational filter transfer function;

wherein the following steps are performed iteratively:

(b1) determining a plurality of intermediate signals from the input signal using the first and second order rational transfer functions and one or more previous intermediate signals determined in a preceding clock cycle of the clock signal;

(b2) adding the plurality of intermediate signals to generate at least one filter output signal wherein the filter output signal corresponds to the rational filter transfer function.

2. The method of claim 1,
wherein (b2) further comprises determining each of the plurality of intermediate signals in parallel and contemporaneously.

3. The method of claim 1,
wherein (b1) further comprises determining each of the plurality of intermediate signals in two clock cycles.

4. The method of claim 1,
wherein at least some of the plurality of intermediate signals are complex signals having real and imaginary parts.

5. The method of claim 1,
wherein at least one of the first and second order rational functions includes a real negative pole or a pair of complex conjugate poles.

6. A digital recursive filter arrangement for filtering an input signal according to a rational filter transfer function comprising:

(a) a first input for receiving the input signal;

(b) a second input for receiving a clock signal;

(c) an interface configured to receive filter coefficients from a computation unit, the computation unit defining first and second order rational functions, the first and second order rational functions constituting a partial fraction expansion of the rational filter transfer function, and the computation unit calculating filter coefficients according to the partial fraction expansion;

(d) one or more first programmable recursive digital filter stages of first order clocked by the clock signal, each first programmable recursive digital filter stage operable to determine first intermediate signals from the input signal according to the filter coefficients corresponding to the first order rational functions;

(e) one or more second programmable recursive digital filter stages of second order clocked by the clock signal, each second programmable recursive digital filter stage operable to determine second intermediate signals from the input signal according to the filter coefficients corresponding to the second order rational functions;

(f) a summing unit configured to adding the first and second intermediate signals for providing filter output signal at an

output, the filter output signal corresponding to the rational filter transfer function.

7. The digital recursive filter arrangement of claim 6, wherein the first and second programmable recursive digital filter stages are connected in parallel.

8. The digital recursive filter arrangement of claim 6, wherein the computation unit further receives the filter output signal, the computation unit operable to determine new filter coefficients as a function of the output signal.

9. The digital recursive filter arrangement of claim 6, wherein the computation unit comprises a memory device coupled to the interface for providing the filter coefficients for the first and second programmable recursive digital filter stages.

10. The digital recursive filter arrangement of claim 6, wherein the first and second first programmable recursive digital filter stages and the summing unit cooperate to generate the filter output signal in two clock cycles.

11. The digital recursive filter arrangement of claim 6, further comprising one delay element in a signal path between the input and the output.

12. The digital recursive filter arrangement of claim 6, wherein each of the first programmable recursive digital filter stages clocked by the clock signal comprises:

- a first multiplier for multiplying the input signal by a first multiplication coefficient;

- a first adder for adding the output signal of the first multiplier and a recursive signal for providing the intermediate signal;

wherein the recursive signal is provided by a second adder, a delay element and a second multiplier having a second multiplication coefficient connected in series, said second adder adding the intermediate signal and the output signal of the first multiplier; and

wherein the multiplication coefficients are programmed according to a recursive convolution in the time domain.

13. The digital recursive filter arrangement of claim 6, wherein each of the second programmable recursive digital filter stages clocked by the clock signal comprises:

- a first node for receiving the input signal;

- a first delay element connected between the first node and a second node;

- a first adder for adding the input signal that is multiplied by a first multiplier having a first multiplication coefficient and the signal from the first delay element said signal being multiplied by a second multiplier having a second multiplication coefficient;

- a second adder for adding the input signal that is multiplied by a third multiplier having a third multiplication coefficient and the signal from the first delay element said signal being multiplied by a fourth multiplier having a fourth multiplication coefficient;

- a third adder for adding the output signal of the first adder, a first and a second recursive signal for providing a first signal at a third node;

- a fourth adder for adding the output signal of the second adder, a third and a fourth recursive signal for providing a second signal at a fourth node; and

- a ninth multiplier for multiplying the second signal by a ninth multiplication coefficient for providing the intermediate signal;

wherein:

- the first recursive signal is provided by the output signal of a second delay element connected at the fourth node, said output signal being multiplied by a fifth multiplier having a fifth multiplication coefficient;

- the second recursive signal is provided by the output signal of a third delay element connected to the third node, said output signal being multiplied by a sixth multiplier having a sixth multiplication coefficient;

- the third recursive signal is provided by the output signal of the second delay element said output signal being multiplied by a seventh multiplier having a seventh multiplication coefficient; and

- the fourth recursive signal is provided by the output signal of the third delay element said output signal being multiplied by an eighth multiplier having an eighth multiplication coefficient; and

wherein the multiplication coefficients are programmed according to a recursive convolution in the time domain.

14. A digital recursive filter arrangement for filtering an input signal according to a partial fraction expansion representation of a rational filter transfer function, the partial fraction expansion being a sum of first and second

order rational functions to be used as first and second order intermediate filter transfer functions, the arrangement comprising:

(a) a first input for receiving the input signal;

(b) a second input for receiving a clock signal;

(c) one or more first recursive digital filter stages of first order clocked by the clock signal, the one or more first recursive digital filter stages configured to determine first intermediate signals according to the first order intermediate filter transfer functions from the input signal using a discrete recursive convolution in the time domain;

(d) one or more second recursive digital filter stages of second order clocked by the clock signal, the one or more second recursive digital filter stages configured to determine second intermediate signals according to the second order intermediate filter transfer functions from the input signal using a second discrete recursive convolution in the time domain;

(e) a summing unit operably coupled to add the intermediate signals of the first and second filter stages and provide a filter output signal at an output, the filter output signal corresponding to the rational filter transfer function.

15. A digital filter stage of first order for filtering an input signal and providing a filter output signal comprising:

- a first multiplier operable to multiply the input signal by a first multiplication coefficient;

- a first adder operable to add the output signal of the first multiplier and a recursive signal and provide the filter output signal;

- a combination of a second adder, a delay element and a second multiplier having a second multiplication coefficient connected in series, said second adder adding the filter output signal and the output signal of the first multiplier to generate a second adder output, the delay element delaying the second adder output, the second multiplier receiving the delayed second adder output and generating the recursive signal therefrom.

16. A digital filter stage of second order for filtering an input signal and providing a filter output signal comprising:

- a first node for receiving the input signal;

- a first delay element connected between the first node and a second node;

- a first adder for adding the input signal that is multiplied by a first multiplier having a first multiplication coefficient and the signal from the first delay element said signal being multiplied by a second multiplier having a second multiplication coefficient;

- a second adder for adding the input signal that is multiplied by a third multiplier having a third multiplication coefficient and the signal from the first delay element said signal being multiplied by a fourth multiplier having a fourth multiplication coefficient;

- a third adder for adding the output signal of the first adder, a first and a second recursive signal for providing a first signal at a third node;

- a fourth adder for adding the output signal of the second adder, a third and a fourth recursive signal for providing a second signal at a fourth node; and

- a ninth multiplier for multiplying the second signal by a ninth multiplication coefficient for providing the filter output signal;

wherein:

- the first recursive signal is provided by the output signal of a second delay element connected at the fourth node, said output signal being multiplied by a fifth multiplier having a fifth multiplication coefficient;

- the second recursive signal is provided by the output signal of a third delay element connected to the third node, said output signal being multiplied by a sixth multiplier having a sixth multiplication coefficient;

- the third recursive signal is provided by the output signal of the second delay element said output signal being multiplied by a seventh multiplier having a seventh multiplication coefficient; and

- the fourth recursive signal is provided by the output signal of the third delay element said output signal being multiplied by an eighth multiplier having an eighth multiplication coefficient.

17. The digital filter stage of claim 15,
wherein the multiplication coefficients correspond to a recursive convolution in the time domain.

18. The digital filter stage of claim 15,
wherein the multiplication coefficients are programmable.

19. The digital filter stage of claim 15,
wherein the delay elements comprise memory cells.

20. The digital filter stage of claim 15, wherein the delay elements, multipliers and adders are clocked by a clock signal.

21. The digital filter stage of claim 16, wherein the multiplication coefficients correspond to a recursive convolution in the time domain.

22. The digital filter stage of claim 16, wherein the multiplication coefficients are programmable.

23. The digital filter stage of claim 16, wherein the delay elements comprise memory cells.

24. The digital filter stage of claim 16, wherein the delay elements, multipliers and adders are clocked by a clock signal.